WHAT IS CLAIMED IS:

1. A circuit, comprising:

at least one memory cell having first and second p-channel transistors and first and second n-channel transistors in a cross-coupled latch configuration; and

power control circuitry coupled to a source terminal of one of the n-channel transistors for providing to that source terminal a low voltage reference level during a normal mode of operation and transitioning that source terminal to a high voltage reference level and back to the low voltage reference level during a data corruption mode of operation.

2. The circuit of claim 1 wherein the source terminal of the other n-channel transistor is always coupled to the low voltage reference.

3. A circuit, comprising:

a memory array comprising a plurality of memory cells, the plurality of memory cells arranged in a plurality of groups, each memory cell having first and second p-channel transistors and first and second n-channel transistors in a cross-coupled latch configuration; and

power control circuitry selectively coupled, one group at time, to source terminals of the n-channel transistors in the selected group, for providing to those source terminals a low voltage reference level during a normal mode of operation and transitioning those source terminals to a high voltage reference level and back to the low voltage reference level during a data corruption mode of operation.

4. The circuit of claim 3 wherein the power control circuitry includes counter circuitry to sequentially select each group of memory cells so as to corrupt all memory cells in the memory array.

5. The circuit of claim 3 wherein the source terminal of the other n-channel transistor in each memory cell is always coupled to the low voltage reference.

6. A circuit, comprising:

a memory cell having first and second p-channel transistors and first and second n-channel transistors in a cross-coupled latch configuration; and

power control circuitry:

a) coupled to a source terminal of at least one of the p-channel transistors for providing to that source terminal a high voltage reference level during a normal mode of operation and transitioning that source terminal to a low voltage reference level and back to the high voltage reference level during a data corruption mode of operation; and

b) coupled to a source terminal of one of the n-channel transistors for providing to that source terminal the low voltage reference level during the normal mode of operation and transitioning that source terminal to the high voltage reference level and back to the low voltage reference level during a data corruption mode of operation.

7. The circuit of claim 6 wherein the source terminal of the other n-channel transistor is always coupled to the low voltage reference.

8. The circuit of claim 6 wherein the power control circuitry transitions voltage on the source terminal of the at least one p-channel transistor and transitions voltage on the source terminal of the n-channel transistor in an interleaved manner.

9. A method for clearing a volatile memory cell, comprising:

transitioning a low voltage reference terminal for a memory cell from a low reference voltage associated with a normal mode of operation to a high reference voltage in a data corruption mode of operation; and

transitioning the low voltage reference terminal from the high reference voltage back to the low reference voltage.

10. The method of claim 9 wherein the memory cell comprises a 6T memory cell and the low voltage reference terminal comprises a source terminal of one n-channel transistor in a latch portion of the memory cell.

11. The method of claim 10 further comprising holding a source terminal of another n-channel transistor in the latch portion of the memory cell at the low reference voltage.

12. The method of claim 10 wherein the volatile memory cell is part of a memory array including a plurality of like volatile memory cells, the volatile memory cells arranged in a plurality of groups, the steps of transitioning comprising selectively transitioning, one group at time, the low voltage reference terminals for the memory cells in the selected group.

13. A circuit, comprising:

a volatile memory cell having a low voltage reference terminal; and

power control circuitry coupled to the volatile memory cell that transitions the low voltage reference terminal from a low reference voltage associated with a normal mode of operation to a high reference voltage in a data corruption mode of operation and transitions the low voltage reference terminal from the high reference voltage back to the low reference voltage.

14. The circuit of claim 13 wherein the volatile memory cell comprises a 6T memory cell and the low voltage reference terminal comprises a source terminal of one n-channel transistor in a latch portion of the memory cell.

15. The circuit of claim 14 wherein a source terminal of another n-channel transistor in the latch is always coupled to the low reference voltage.

16. The circuit of claim 13 further comprising a memory array including a plurality of volatile memory cells, the memory cells arranged in a plurality of groups, the power control circuitry selectively transitioning, one group at time, the low voltage reference terminals for the memory cells in the selected group.

17. A method for clearing a volatile memory cell, comprising:

transitioning a high voltage reference terminal for a volatile memory cell from a high reference voltage associated with a normal mode of operation to a low reference voltage in a data corruption mode of operation, and then returning the high voltage reference terminal back to the high reference voltage; and

transitioning a low voltage reference terminal for the volatile memory cell from the low reference voltage associated with the normal mode of operation to the high reference voltage in a data corruption mode of operation, and then returning the low voltage reference terminal back to the low reference voltage.

18. The method of claim 17 wherein the memory cell comprises a 6T memory cell and the low voltage reference terminal comprises a source terminal of one n-channel transistor in a latch portion of the memory cell and the high voltage reference terminal comprises a source terminal of at least one p-channel transistor in the latch portion of the memory cell.

19. The method of claim 18 further comprising holding a source terminal of another n-channel transistor in the latch portion of the memory cell at the low reference voltage.

20. The method of claim 17 wherein the volatile memory cell is part of a memory array including a plurality of like volatile memory cells, the steps of transitioning comprising transitioning the low voltage reference terminals and high voltage reference terminals for all the memory cells.

21. The method of claim 17 wherein the steps of transitioning voltage on the low and high voltage reference terminals are performed in an interleaved manner.

22. A circuit, comprising:

a volatile memory cell having a low voltage reference terminal and a high voltage reference terminal; and

power control circuitry coupled to the volatile memory cell that transitions:

a) the high voltage reference terminal from a high reference voltage associated with a normal mode of operation to a low reference voltage in a data corruption mode of operation and back to the high reference voltage; and

b) the low voltage reference terminal from a low reference voltage associated with a normal mode of operation to a high reference voltage in a data corruption mode of operation and back to the low reference voltage.

23. The circuit of claim 22 wherein the volatile memory cell comprises a 6T memory cell and the low voltage reference terminal comprises a source terminal of one n-channel transistor in a latch portion of the memory cell and the high voltage reference terminal comprises a source terminal of at least one p-channel transistor in the latch portion of the memory cell.

24. The circuit of claim 23 wherein a source terminal of another n-channel transistor in the latch is always coupled to the low reference voltage.

25. The circuit of claim 22 wherein the volatile memory cell is part of a memory array including a plurality of like volatile memory cells, the power control circuitry transitioning

the low voltage reference terminals and high voltage reference terminals for all the memory cells.

26. The circuit of claim 22 wherein the power control circuitry transitions voltage on the low and high voltage reference terminals in an interleaved manner.

27. A circuit, comprising:

a memory array comprising a plurality of memory cells, each memory cell having first and second p-channel transistors and first and second n-channel transistors in a cross-coupled latch configuration; and

power control circuitry:

a) coupled to a source terminal of at least one of the p-channel transistors in each of the memory cells within the memory array for providing to those source terminals a high voltage reference level during a normal mode of operation and transitioning those source terminals to a low voltage reference level and back to the high voltage reference level during a data corruption mode of operation; and

b) coupled to a source terminal of one of the n-channel transistors in each of the memory cells within the memory array for providing to those source terminal the low voltage reference level during the normal mode of operation and transitioning those source terminals to the high voltage reference level and back to the low voltage reference level during a data corruption mode of operation.

28. The circuit of claim 27 wherein the source terminal of the other n-channel transistor in each of the memory cells within the memory array is always coupled to the low voltage reference.

29. The circuit of claim 27 wherein the power control circuitry transitions voltage on the source terminal of the at least one p-channel transistor and transitions voltage on the source terminal of the n-channel transistor in each of the memory cells within the memory array in an interleaved manner.